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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. <b>211.001-D4-US</b>	SERIAL NUMBER <b>10/727,742</b>
	APPLICANT(S) <b>Fazan et al.</b>	
	FILING DATE <b>December 4, 2003</b>	GROUP ART UNIT

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>JH</i>	4,032,947	6/1977	Kesel et al.	257	214	
<i>JH</i>	3,997,799	12/1976	Baker	365	183	
<i>JH</i>	5,448,513	9/1995	Hu et al.	365	150	
<i>JH</i>	4,298,962	11/1981	Hamano et al.	365	182	
<i>JH</i>	3,439,214	4/1969	Kabell	315	11	
<i>JH</i>	6,081,443	6/2000	Morishita	365	149	
<i>JH</i>	6,111,778	8/2000	MacDonald et al.	365	149	

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<i>JH</i>	FR 2 197 494	3/1974	French			
<i>JH</i>	EP 1 180 799	2/2002	European			
<i>JH</i>	EP 0 030 856	6/1981	European			
<i>JH</i>	GB 1 414 228	11/1975	Great Britain			
<i>JH</i>	EP 0 694 977	1/1996	European			
<i>JH</i>	JP 02 294076	2/1991	Japanese			
<i>JH</i>	EP 1 237 193	9/2002	European			
<i>JH</i>	EP 0 878 804	11/1998	European			

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<i>JH</i>	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382

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<i>JE</i>	5,936,265	8/1999	Koga	257	105	
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<i>JE</i>	EP 0 801 427	10/1997	European			
<i>JE</i>	EP 0 513 923	11/1992	European			

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JH	"Toshiba's DRAM Cell Piggybacks on SOI Wafer", Y. Hara, EE Times, June 2003

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JM	"An SOI 4 Transistors Self-Refresh Ultra-Low-Voltage Memory Cell", Thomas et al., IEEE, March 2003, pp.401-404
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<i>JH</i>	"Dynamic Effects in SOI MOSFET's", Giffard et al., IEEE, 1991, pp.160-161
<i>JH</i>	"A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs", Fazan et al., IEEE 2002 Custom Integrated Circuits Conference, June 2002, pp.99-102
<i>JH</i>	"A Novel Pattern Transfer Process for Bonded SOI Giga-bit DRAMs", Lee et al., Proceedings 1996 IEEE International SOI Conference, Oct. 1996, pp.114-115
<i>JH</i>	"An Experimental 2-bit/Cell Storage DRAM for Macrocell or Memory-on-Logic Application", Furuyama et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 2, April 1989, pp.388-393
<i>JH</i>	"High-Performance Embedded SOI DRAM Architecture for the Low-Power Supply", Yamauchi et al., IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp.1169-1178
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JM	"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application", Wann et al., IEEE Electron Device Letters, Vol. 16, No. 11, November 1995, pp.491-493
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JM	"Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI", Assaderaghi et al., IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pp.414-422
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